

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Cho et al.

Atty Docket No.: NOVLP089/NVLS-
002886/002887

Application No.: 10/800,377

Examiner: Not yet assigned

Filed: March 11, 2004

Group: 2812

Title: METHOD AND APPARATUS FOR UV
EXPOSURE OF LOW DIELECTRIC
CONSTANT MATERIALS FOR POROGEN
REMOVAL AND IMPROVED MECHANICAL
PROPERTIES

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on June 20, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____

Tara Hayden

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

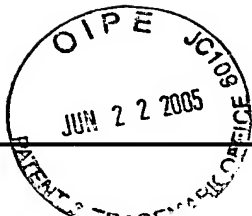
This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NOVLP089).

Respectfully submitted,

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	Applicant: Cho et al.	
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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	6,387,453	05.14.02	Brinker et al.			
	A2	5,789,027	08.04.98	Watkins et al.			
	A3	6,391,932 B1	05.21.02	Gore et al.			
	A4	5,700,844	12.23.97	Hedrick et al.			
	A5	2003/0157248 A1	08.21.03	Watkins et al.			
	A6	2002/0123240 A1	09.05.02	Gallagher et al.			
	A7	6,340,628	01.22.02	Van Cleemput, et al.			
	A8	6,383,955	05.07.02	Matsuki, et al.			
	A9	6,596,654	07.22.03	Bayman, et al.			
	A10	2004/0099952	05.27.04	Goodner et al.			
	A11	2004/0102031	05.27.04	Kloster et al.			
	A12	2004/0185679	09.23.04	Ott et al.			
	A13	6,848,458	02.01.05	Shrinivasan et al.			
	A14	6,805,801	10.19.04	Humayun et al.			
	A15	6,391,932	05.21.02	Gore et al.			
	A16	4,882,008	11.21.89	Garza et al.			
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	A18	6,268,276	07.31.01	Chan et al.			
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	A24	6,312,793	11.06.01	Grill et al.			
	A25	6,576,345	06.10.03	Cleemput et al.			
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	A31	2004/0069410	04.2004	Moghadam et al.			
	A32	6,756,085	06.29.04	Waldfried et al.			
Examiner				Date Considered			

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B1	WO95/07543	03.16.95	WIPO			X	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	Jan, C.H., et al, <i>90NM Generation, 300mm Wafer Low k ILD/Cu Interconnect Technology</i> , 2003 IEEE Interconnect Technology Conference.
	C2	Wu et al., U.S. Application No. 10/789,103 (Atty Docket No.: NOVLP094), entitled: Methods For Producing Low-K CDO Films With Low Residual Stress
	C3	Wu et al., U.S. Application No. 10/820,525 (Atty Docket No.: NOVLP091), entitled: Methods For Producing Low-K CDO Films With Low Residual Stress
	C4	Wu et al., U.S. Application No. 10/800,409 (Atty Docket No.: NOVLP098), entitled: Methods For Producing Low-K CDO Films
	C5	U.S. Patent Application No. 10/016,017, File Date: December 12, 2001 (Atty Dkt: NOVLP030)
	C6	U.S. Patent Application No. 10/125,614, File Date: April 18, 2002 (Atty Dkt: NOVLP028)
	C7	U.S. Patent Application No. 10/202,987, File Date: July 23, 2002 (Atty Dkt: NOVLP028X1)
	C8	Tipton et al., "Method for Removal of Porogens From Porous Low-K Films Using Supercritical Fluids", Novellus Systems, Inc., Application No. 10/672,305, filed 9/26/03, pages 1-32. Atty. Docket No. NOVLP069/NVLS-000821
	C9	Humayun et al., "Method For Forming Porous Films By Porogen Removal Combined With In Situ Modification", U.S. Patent No. 10/404,693, filed March 31, 2003, Office Action dated March 15, 2005 (Atty Dkt: NOVLP064)
	C10	Tipton et al., "Method Of Porogen Removal From Porous Low-K Films Using UV Radiation", U.S. Application No. 10/672,311, filed September 26, 2003, Office Action dated September 7, 2004 (Atty Dkt: NOVLP075/NVLS-000820)
	C11	Tipton et al., "Method Of Porogen Removal From Porous Low-K Films Using UV Radiation", U.S. Application No. 10/672,311, filed September 26, 2003, Office Action dated December 28, 2004 (Atty Dkt: NOVLP075/NVLS-000820)
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	C12	Tipton et al., "Method For Removal Of Porogens From Porous Low-K Films Using Supercritical Fluids", U.S. Patent No. 10/672,305, Office Action dated March 22, 2005 (Atty Dkt: NOVLP069).
	C13	R.D. Miller et al., "Phase-Separated Inorganic-Organic Hybrids for Microelectronic Applications," MRS Bulletin, October 1997, Pages 44-48
	C14	Jin et al., "Nanoporous Silica as an Ultralow- <i>k</i> Dielectric," MRS Bulletin, October 1997, Pages 39-42
	C15	Asoh et al., "Fabrication of Ideally Ordered Anodic Porous Alumina with 63 nm Hole Periodicity Using Sulfuric Acid," J. Vac. Sci. Technol. B 19(2), Mar/Apr 2001, Pages 569-572
	C16	Asoh et al., "Conditions for Fabrication of Ideally Ordered Anodic Porous Alumina Using Pretextured Al," Journal of the Electrochemical Society, 148 (4) B152-B156 (2001) Pages B152-B156
	C17	Holland et al., "Nonlithographic Technique for the Production of Large Area High Density Gridded Field Sources," J. Vac. Sci. Technol. B 17(2), Mar/Apr. 1999, Pages 580-582
	C18	Masuda et al. "Highly Ordered Nanochannel-Array Architecture in Anodic Alumina," App. Phys. Lett. 71(19), November 1997, Pages 2770-2772
	C19	Clube et al., "White Paper from Holotronic Technologies SA; downloaded from www.hdotronic.com/whitepaper/fine-patt.pdf on March 12, 2002
	C20	Meli et al., "Self-Assembled Masks for the Transfer of Nanometer-Scale Patterns into Surfaces: Characterization by AFM and LFM", Nano Letters, Vol. 2, No. 2, 2002, 131-135
	C21	"Shipley Claims Porous Low K Dielectric Breakthrough," Press Release March 17, 2003.
	C22	Jeffrey M. Calvert and Michael K. Gallagher, Semiconductor International, 26 (12), 56 (2003).
	C23	Van Bavel et al., Future Fab International, 16, (2004).
	C24	Caluwaerts et al, "Post Patterning Meso Porosity Creation: A Potential Solution For Pore Sealing," IITC 2003.
	C25	Peter Singer, "New Materials and Designs to Improve Transistor Performance", April 1, 2004, Semiconductor International.
	C26	Ghani et al, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors", IEEE, © 2003.
	C27	Bhadri N. Varadarajan, "Tensile Silicon Nitride – P1264 NESL", C & F Study, August 21, 2003.
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	C28	Varadarajan, et al., "Strained Transistor Architecture and Method", Novellus Systems, Inc., Appln No. 10/923,259, filed August 20,2004, pages 1-24. [Atty Docket No. NOVLP108/NVLS-2933].
	C29	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, filed June 2, 2004, (Atty Dkt: NOVLP099)
	C30	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, Office Action dated March 2, 2005, (Atty Dkt: NOVLP099)
	C31	Niu et al., "Methods For Improving The Cracking Resistance Of Low-K Dielectric Materials", U.S. Application No. 10/860,340, Final Office Action dated June 13, 2005, (Atty Dkt: NOVLP099)
	C32	Wang et al., "Plasma Detemplating And Silanol Capping Of Porous Dielectric Films", U.S. Application No. 10/785,235, filed February 23, 2004 (Atty Dkt: NOVLP085)
	C33	Varadarajan et al., "Tensile Dielectric Films Using UV Curing", U.S. Application No. 10/972,084, filed October 22, 2004 (Atty Dkt: NOVLP122)
	C34	Fox et al., "Method For Improving Mechanical Properties Of Low Dielectric Constant Materials", U.S. Application No. 10/849,568, filed May 18, 2004 (Atty Dkt: NOVLP083)
	C35	Fox et al., "Methods For Producing Low-Stress Carbon-Doped Oxide Films With Improved Integration Properties", U.S. Application No. 10/987,208, filed November 12, 2004 (Atty Dkt: NOVLP104)
	C36	Van Den Hoek et al., "VLSI Fabrication Processes For Introducing Pores Into Dielectric Materials," U.S. Application No. 11/050,621, filed January 31, 2005 (Atty Dkt: NOVLP100)
	C37	Draeger et al., "Creation Of Porosity In Low-K Films By Photo-Disassociation Of Imbedded Nanoparticles," U.S. Application No. 11/146,456, filed June 6, 2005 (Atty Dkt: NOVLP100X1)
	C38	Wu et al., "Methods For Producing Low Stress Porous Low-K Dielectric Materials Using Precursors With Organic Functional Groups", U.S. Application No. 10/927,777, filed August 27, 2004 (Atty Dkt: NOVLP106)
	C39	Wu et al., "Methods For Improving Integration Performance Of Low Stress CDO Films", U.S. Application No. 10/941,502, filed September 14, 2004 (Atty Dkt: NOVLP107)
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	C40	Cho et al., "Methods of Improving Porogen Removal and Film Mechanical Strength in Producing Ultra Low-K Carbon Doped Oxide Films Using Radical Photopolymerization", U.S. Application No. 10/982,654, filed November 5, 2004 (Atty Dkt: NOVLP115)
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